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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/645,330	08/21/2003	Richard C. Foss	2037.1004-007	7565
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21005	7590	11/12/2004
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EXAMINER

TRAN, MICHAEL THANH

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,330	FOSS ET AL.	
	Examiner	Art Unit	
	Michael t Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-69 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 50-69 is/are allowed.
- 6) ☒ Claim(s) 18-21, 29, 33, 34 and 49 is/are rejected.
- 7) ☒ Claim(s) 22-28, 30-32 and 35-48 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.



Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In response to the Communications dated August 26, 2004, claims 18-69 are active in this application as a result of the cancellation of claims 1-17 and addition of claims 18-69.

Claim Objections

2. Claims 22, 23, 24-28, 30-32, 35-48, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It appears that the word "though", in claim 24, line 2, should be changed to – through--.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the

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purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 18-21 and 29 are rejected under 35 U.S.C 102(b) as being anticipated by Ware et al. [U.S. Patent #5,337,285].

With respect to claim 18, Ware et al. disclose a synchronous memory comprising: a clock input signal; and a delayed locked loop [DLL] having an adjustable delay line for generating a driving clock signal from the clock input signal, the DLL being enabled and disabled by external control. *See second paragraph of the "Summary of The Invention" section. In the cited section, Ware et al. state that there exists an external clock input from which the delayed locked loop synthesizes an internal clock which is used to drive loads. The delayed locked loop is being controlled by external control via element 180 of figure 2.*

With respect to claim 19, Ware et al. disclose that the DLL is disabled during a standby state. See the seventh paragraph of the "Detailed Description of the Invention" section. In the cited section, Ware et al. state that the DLL exists from the standby mode to full operation with one latch and buffer delay.

With respect to claim 20, Ware et al. disclose that the device further comprising a clock buffer coupled with the clock input signal for generating a buffered clock signal, the buffered clock signal being used when the DLL is disabled. *See second paragraph of the "Summary of The Invention" section, the seventh paragraph of the "Detailed Description of the Invention" section, and figure 2.*

With respect to claim 21, Ware et al. disclose that the settings of the delay line are maintained when the DLL is disabled. See the eighth paragraph of the "Detailed Description of the Invention" section. In the cited section, Ware et al. state that the feedback loop is not disturbed during the disable phase.

With respect to claim 29, Ware et al. disclose a data output buffer [140] enabled by the driving clock signal for outputting data to an output terminal. See figure 2.

5. Claim 33 is rejected under 35 U.S.C 102(b) as being anticipated by Harness et al. [U.S. Patent #5,479,647].

With respect to claim 33, Harness et al. disclose a synchronous dynamic random access memory comprising: a clock input signal [output of element 25 of figure 3]; a delay locked loop [DLL] having an adjustable delay line [41 of figure 1] for generating a driving clock signal from the clock input signal, the DLL being enabled and disabled by external control [power on/off]. See 28th paragraph of the "Detailed Description" section. In the cited section, Harness et al. indicated that the delay circuit 41 has a controllable delay.

6. Claim 34 is rejected under 35 U.S.C 102(b) as being anticipated by Harness et al. [U.S. Patent #5,479,647].

With respect to claim 34, Harness et al. disclose a method of providing a clock to a synchronous memory comprising: generating a driving clock signal [output of 41 of figure 3] from a clock input signal [via element 25 of figure 3] through a delay locked

loop [DLL] [element 41 of figure 3] having an adjustable delay line; and using external control, disabling the delay locked loop [power on/off]. See 28th paragraph of the "Detailed Description" section. In the cited section, Harness et al. indicated that the delay circuit 41 has a controllable delay.

7. Claim 49 is rejected under 35 U.S.C 102(b) as being anticipated by Harness et al. [U.S. Patent #5,479,647].

With respect to claim 49, Harness et al. disclose a synchronous memory comprising: means for generating a driving clock signal [40 via 41 of figure 3] from a clock input signal [25 of figure 3] through a delay locked loop [DLL] [41 of figure 3] having an adjustable delay line; and means for disabling the delay locked loop by external control [power on/off]. See 28th paragraph of the "Detailed Description" section. In the cited section, Harness et al. indicated that the delay circuit 41 has a controllable delay.

Allowable Subject Matter

8. Claims 50-69 are allowable over the prior art of record.

9. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- ❖ Wherein the settings are maintained during power down.
- ❖ Wherein the settings are maintained during a standby state.

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- ❖ Comprising a delay comparator coupled to the adjustable delay line for setting the delay through the delay line, the comparator having a first input coupled to the clock input signal and a second input coupled to the driving clock signal.
- ❖ Wherein the adjustable delay line is a tapped delay line.
- ❖ Wherein the DLL is enabled and disabled by a register bit.
- ❖ Wherein the DLL is enabled and disabled by register data.
- ❖ Wherein the DLL is enabled and disabled by a register.
- ❖ Circuitry that receives the driving clock signal when the DLL is enabled and receives the buffered clock signal when the DLL is disabled.

Remarks

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date

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of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Conclusion

11. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

13. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.



Michael T. Tran
Art Unit 2818
November 9, 2004